REMARKS

Claims 1, 4-5, 17-18, 21-22, 24, 27-28, 32, 40-41, 45, 47, 52-53, 60, 64-66, 68-70, 73, 76-78, 85, and 88-89 have been amended. Claims 3, 7, 15, 20, 26, 30,38, 43, 48-50, 59, 61-63, 67, 72, 75, 82, 87, and 95 have been canceled. Claims 97-100 have been added. Claims 1-2, 4-14, 16-19, 21-25, 27-37, 39-42, 44-47, 51-58, 60, 64-71, 73-74, 76-81, 83-86, 88-94, and 96-100 are pending.

The abstract and title of the invention has been amended to better describe the invention.

Applicants' representative is grateful for the indication that claims 14, 31-32, 37, 45-46, 58, 65-66, 71, 84, 90, and 96 have been allowed. However, as each of these claims depend from at least one rejected base claim, applicants' representative is assuming that these claims are recite allowable subject matter and stand objected to as being dependent upon their respective rejected base and/or intervening claims.

Claim 3 and 26 stand objected to due to the use of the phrase "memory block to be erased." Claims 3 and 26 have been canceled, thus, this objection should be withdrawn.

Claims 8-9, 22-23, 52-53, and 77-78 stand rejected under 35 U.S.C. § 112, first paragraph. This rejection is respectfully traversed. The Office Action alleges that the specification does not support the division of data regions into pieces for the refreshing step. The specification describes the memory device as comprising a plurality of main blocks, with each main block comprising a plurality of erase blocks, with each erase block being further subdivided, for example, into a plurality of sectors. See, e.g., specification at paragraph [0002]. The specification therefore discloses dividing data. When multiple data items require refreshing, the specification also discloses that the

data items can be refreshed over a span of time interrupted by other operations. See, e.g., paragraph [0032]. Accordingly, the rejection claims 8-9, 22-23, 52-53, and 77-78 under 35 U.S.C. § 112, first paragraph should be withdrawn.

Claims 50 and 76 stand rejected under 35 U.S.C. § 112, first paragraph. This rejection is respectfully traversed. Restoration of the contents of a memory block to the same memory block is disclosed in the specification at, for example, paragraph [0033] with respect to system data. Accordingly, the rejection of claims 50 and 76 under 35 U.S.C. § 112, first paragraph should be withdrawn.

Claims 15, 38, 59, 72, 82, and 95 stand rejected under 35 U.S.C. § 112, first paragraph. Claims 15, 38, 59, 72, 82, and 95 have been canceled.

Claims 21-23, 27, and 75-76 stand rejected under 35 U.S.C. § 112, second paragraph for various informalities. Claim 75 has been canceled. Claims 21-22, and 76 have been amended to provide proper antecedent basis. Claim 27 has been amended to depend from claim 26. Accordingly, the rejection to claims 21-23, 27, and 75-76 should be withdrawn.

Claims 1-7, 10-12, 17-21, 47-51, 54-56, 73-75, 79-81 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Norman (U.S. Patent No. 5,715,193). Claims 24-30, 33-35, 39-45, 60-64, 67-69, 85-88, and 91-93 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Norman. Claims 18-21 and 41-44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Norman in view of Kon (U.S. Patent No. 6,249,838). Claims 13, 36, 57, 70, 83, and 95 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Norman in view of Bruce (U.S. Patent No. 6,000,006). These rejections are respectfully traversed.

Claims 1 and 97 recite, *inter alia,* "when a counter equals or exceeds a predetermined threshold value, always refreshing the data in the memory block associated with said counter by: storing data from the memory block associated with said counter in another one of said memory blocks."

Claims 17 recites, *inter alia,* "for each counter which equal or exceed a second predetermined value, always refreshing a memory block associated with said counter by storing data contained in said memory block in a different memory block of said flash memory array."

Claim 18 recites, *inter alia,* "for each counter which is less than or equal to a second predetermined value, always refreshing a memory block associated with said counter by storing data contained in said memory block in a different memory block of said flash memory array."

Claims 24 and 98 recite, *inter alia,* "always refreshing the data in a sector of the one memory block of said ... array when an associated counter equals or exceeds a predetermined threshold value by storing data contained in that sector to different sector.

Claim 40 recites, *inter alia,* "always refreshing all sectors that have associated counters which equal or exceed a second predetermined value by storing data from a sector in a different sector in said flash memory array."

Claim 41 recites, *inter alia,* "always refreshing all sectors that have associated counters which are less than or equal to a second predetermined value by storing data from a sector in a different sector in said flash memory array."

Claims 47 and 99 recite, *inter alia,* "wherein when one of said plurality of counter values equals or exceeds a predetermined threshold value, said control circuit always refreshes the data in the memory block associated with said counter by storing the data stored in said memory block in a different memory block."

Claims 60 and 100 recite, *inter alia,* "wherein when one of said plurality of counters equals or exceeds a predetermined threshold value, said control circuit always refreshes the data in the sector associated with said counter by storing the data stored in said sector in a different sector."

Claim 73 recites, *inter alia,* "wherein when one of said plurality of counters equals or exceeds a predetermined threshold value, the data in the memory storage region associated with said counter is always refreshed by storing data of said memory storage region in a different memory storage region."

Claim 85 recites, *inter alia,* "wherein when one of said plurality of counters equals or exceeds a predetermined threshold value, the data in the sector associated with said counter is always refreshed by storing the data stored in said sector to a different sector."

Norman discloses a flash memory system in which a controller maintains a table of counter values, each respectively associated with a portion of the flash memory. When a portion of the flash memory is written, the counter associated with the portion of the flash memory is reset to zero, while the counters associated with the non-written portions of the flash memory are incremented. When any counter value exceeds a threshold, Norman discloses the associated portion of the flash memory is "refreshed."

The refreshing performed by Norman is illustrated by, for example, Fig. 4A. Essentially, data from the portion being refreshed is read to determine whether error

correction is required to properly read the data. Fig. 4A, step 214. If error correction is not required, the associated counter is set to a new value and the refresh operation is completed. Fig. 4A, steps 216-218.

In contrast, the independent claims, as amended, each require, when a counter has reached a threshold, data from the portion of the flash memory associated with the counter to "always" be refreshed by storing that data to another portion of the flash memory. As noted above, Norman does not disclose or suggest this feature of the invention.

The Office Action additionally cites to Kon, which discloses associating physical medium information in a file system header, and Bruce, which discloses a table for managing remapping and cache-index status information. Neither of these references disclose or suggest the above noted features of the invention.

Accordingly, independent claims 1, 17-18, 24, 40-41, 47, 60, 73, 85, and 97-100 are believed to be allowable over the prior art of record. The depending claims (i.e., claims 2, 4-14, 16, 19, 21-23, 25, 27-37, 39, 42, 44-46, 51-58, 64-71, 74, 76-81, 83-84, 86, 88-94, and 96) are also believed to be allowable for at least the same reasons as the independent claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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